

03/23/01

ISSUE CLASSIFICATION	
Class	Subclass

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<p>O.I.P.E.</p> <p>FA SCANNED HKm[®] Q.A. CH</p>	<p>PATENT DATE</p>
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/816599	F	257	6-1	2826	Sigona

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Semiconductor package including stacked chips

PTO-2040
12/99[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
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